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LEYDIG VOIT & MAYER, LTD
TWO PRUDENTIAL PLAZA, SUITE 4900
180 NORTH STETSON AVENUE
CHICAGO, IL 60601-6780

EXAMINER

LAZARO, DAVID R

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/638,774
Filing Date: August 15, 2000
Appellant(s): PHILLIPS ET AL.

MAILED

JUN 23 2005

Technology Center 2100

Mark Joy (35,562)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/22/2005.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Grounds of Rejection To Be Reviewed on Appeal*

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of the claims under appeal.

| | | |
|-----------|-----------------|---------|
| 5,978,577 | RIERDEN ET AL. | 11-1999 |
| 6,425,056 | BASHAM ET AL. | 07-2002 |
| 5,546,558 | JACOBSON ET AL. | 02-1995 |
| 6,484,186 | RUNGTA | 11-2002 |
| 6,374,296 | LIM ET AL. | 04-2002 |

(9) Grounds of Rejection

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 7, 9, 11, 12, 13, 14, 19, 21, 23 and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Patent 5,978,577 by Rierden et al. (Rierden).

With respect to Claim 1, Rierden teaches a distributed multiprocessor server system for facilitating delegated processing of at least portions of request associated

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with request message received via a communicatively couple network link (Col. 4 lines 15-16), the system comprising:

- a network interface (Col. 4 lines 63-65);

- an intelligent switch couple to the network interface (Col. 9 lines 31-34), the switch comprising logic components for identifying a new request, corresponding to a message packet received by the network interface, passed from the network interface to the intelligent switch (Col. 9 lines 31-34);

- a default handler processor coupled to the intelligent switch (Col. 17 lines 4-5) and configured to receive the new request from the intelligent switch, the default handler processor comprising delegation logic facilitating: associating a request type with at least a portion of the new request (Col. 17 lines 19-21), identifying a handler processor from a set of specialized handler processors for executing at least the portion of the new request based upon the request type (Col. 17 lines 6-8), and issuing a message reassigning at least the portion of the new request to the identified handler processor (Col. 17 lines 6-24 and 43-49);

- and at least one bus structure communicatively linking the set of specialized handler processors to the intelligent switch and request reassignment tracking logic enabling the intelligent switch to route message associated with at least the portion of the reassigned request between the identified processor and the network interface, thereby facilitating completing at least the portion of the new request through communications between the identified handler of specialized handler processors and

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the network interface via the intelligent switch without intervention by the default handler processor (Col. 17 lines 16-24 and 43-49).

With respect to Claim 2, Rierden teaches all the limitations of Claim 1 and further teaches a storage server system is linked to the intelligent switch (Col. 4 line 65 to Col. 5 line 5) via a non-blocking switch (Col. 9 lines 31-34).

With respect to Claim 7, Rierden teaches all the limitations of Claim 2 and further teaches the set of specialized handler processors includes a processor facilitating transfer of a file stored on the storage server system (Col. 9 lines 13-25).

With respect to Claim 9, Rierden teaches all the limitations of Claim 2 and further teaches the set of specialized handler processors includes a processor including functionality facilitating transforming the data within a file prior to a transfer (Col. 8 lines 5-12).

With respect to Claim 11, Rierden teaches all the limitations of Claim 1 and further teaches a data retrieval buffer interposed between a data storage facility and the set of specialized handler processors, the data retrieval buffer being independently accessible with respect to a primary RAM utilized by the default handler processor (Col. 5 lines 2-5).

With respect to Claim 12, Rierden teaches all the limitations of Claim 1 and further teaches new/old request differentiation logic enabling the server system to identify and respond to new connection requests at a different level of priority than a priority assigned to requests associated with existing connections (Col. 9 lines 26-31).

With respect to Claim 13, Rierden teaches a method for allocating received requests in a multiprocessor network server including a network interface, an intelligent switch (Col. 9 lines 31-34), a default handler processor (Col. 17 lines 4-5), and a set of specialized handler processors (Col. 17 lines 7-8), the method comprising the steps of:

receiving, by the network interface, a message packet including a request (Col. 8 lines 62-65);

passing at least the request to the intelligent switch (Col. 8 lines 65-67);

determining the request is a new request, and in response performing the further steps of;

identifying by the default handler processor, based upon a request type of the new request, a handler processor from the set of specialized handler processors that is capable of executing at least a portion of the new request (Col. 17 lines 6-24 and 43-49), and

reassigning by the default handler processor, the new request to the identified handler processor to perform at least a portion of the new request (Col. 17 lines 16-24 and 43-49) wherein the intelligent switch creates a table entry identifying the request and the identified handler processor to which at least a portion of the new request is reassigned (Col. 15 lines 27-39); and

executing, by the identified handler processor, at least the portion of the new request (Col. 7 lines 65-67 and Col. 16 lines 65-67) wherein during executing step the identified handler processor communicates with the network interface via the intelligent

switch, thereby bypassing the default handler processor while executing at least the portion of the new request (Col. 17 lines 40-43).

With respect to Claim 14, Rierden teaches all the limitations of Claim 13 and further teaches a storage server system is linked to the intelligent switch (Col. 4 line 65 to Col. 5 line 5) via a non-blocking switch (Col. 9 lines 31-34), and the executing step comprises transferring data from the storage server to the network interface (Col. 17 lines 46-49).

With respect to Claim 19, Rierden teaches all the limitations of Claim 14 and further teaches within the set of specialized handler processors, a processor facilitating transfer of a file stored on the storage server system (Col. 9 lines 13-25).

With respect to Claim 21, Rierden teaches all the limitations of Claim 14 and further teaches within the set of specialized handler processors, a processor including functionality facilitating transforming the data within a file prior to transfer (Col. 8 lines 5-12).

With respect to Claim 23, Rierden teaches all the limitations of Claim 13 and further teaches storing data retrieved from a data storage facility in a data retrieval buffer interposed between a data storage facility and the set of specialized handler processors, the data retrieval buffer being independently accessible with respect to a primary RAM utilized by the default handler processor (Col. 5 lines 2-5).

With respect to Claim 24, Rierden teaches all the limitations of Claim 13 and further teaches differentiating a new connection request from a request associated with an existing connection, thereby facilitating assigning a first priority to the request

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associated with the existing connection and a second priority to the new connection request (Col. 9 lines 26-31).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rierden in view of U.S. Patent 6,425,059 by Basham et al. (Basham).

With respect to Claim 3, Rierden teaches all the limitations of Claim 2 but does not explicitly disclose the storage server system having memory arranged as a set of version controlled partitions. However it is well known in the art that memory can be arranged into a set of version controlled partitions as shown by Basham (Col. 4 lines 39-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the system disclosed by Rierden and modify it as indicated by Basham with the storage server system comprising memory arranged as a set of version controlled partitions. One would be motivated to have this as it allows one to share data among multiple users without destroying the integrity of the data (Col. 1 lines 33-36 of Basham).

With respect to Claim 15, Rierden teaches all the limitations of Claim 14 but does not explicitly disclose arranging stored content within the system as a set of version

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controlled partitions. However it is well known in the art that memory that can store content can be arranged into a set of version controlled partitions as shown by Basham (Col. 4 lines 39-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the method disclosed by Rierden and modify it as indicated by Basham with the step of arranging stored content within the storage server system as a set of version controlled partitions. One would be motivated to have this as it allows one to share data among multiple users without destroying the integrity of the data (Col. 1 lines 33-36 of Basham).

Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rierden in view of Basham as applied to claims 3 and 15 above, and further in view of U.S. Patent 5,546,558 by Jacobson et al. (Jacobson).

With respect to Claim 4, Rierden in view of Basham teaches all the limitations of Claim 3 but does not explicitly disclose incorporating a straddle into a partition. However, it is well known in the art that a straddle can be incorporated into a partition to facilitate continuous availability of stored data as shown by Jacobson (Col. 8 lines 30-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the system disclosed by Rierden and modify it as indicated by Jacobson wherein a straddle is incorporated into a partition, thereby facilitating continuous availability of all stored data while a particular partition is relocated within the storage server system. One would be motivated to have this as it is desired to have continuous data availability in a storage system (Col. 1 lines 30-40 of Jacobson).

With respect to Claim 16, Rierden in view of Basham teaches all the limitations of Claim 15 but does not explicitly disclose incorporating a straddle into a partition. However, it is well known in the art that a straddle can be incorporated into a partition to facilitate continuous availability of stored data as shown by Jacobson (Col. 8 lines 30-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the method disclosed by Rierden and modify it as indicated by Jacobson wherein a straddle is incorporated into a partition, thereby facilitating continuous availability of all stored data while a particular partition is relocated within the storage server system. One would be motivated to have this as it is desired to have continuous data availability in a storage system (Col. 1 lines 30-40 of Jacobson).

Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rierden in view of U.S. Patent 6,484,186 by Rungta (Rungta).

With respect to Claim 5, Rierden teaches all the limitations of Claim 2 but does not explicitly disclose using a bitmap entry to represent a state of a file maintained by the storage server system. However it is well known in the art that the state of a file maintained in a system can be represented in the form of a bitmap entry as shown by Rungta (Col 1 lines 42-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the system disclosed by Rierden and modify it as indicated by Rungta with a state of a file maintained by the storage server system is represented in the form of a bitmap entry and wherein a first bit is associated with a creator of new data in the file and a second bit is associated with a deleter of data

stored in the file. One would be motivated to have this as it allows for internal file consistency that needs to be maintained in a system (Col. 1 lines 25-26 of Rungta).

With respect to Claim 17, Rierden teaches all the limitations of Claim 14 but does not explicitly disclose using a bitmap entry to represent a state of a file maintained by the storage server system. However it is well known in the art that the state of a file maintained in a system can be represented in the form of a bitmap entry as shown by Rungta (Col 1 lines 42-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the method disclosed by Rierden and modify it as indicated by Rungta with the storage server system maintaining a state of a file in the form of a bitmap entry and wherein a first bit is associated with a creator of new data in the file and a second bit is associated with a deleter of data stored in the file. One would be motivated to have this as it allows for internal file consistency that needs to be maintained in a system (Col. 1 lines 25-26 of Rungta).

Claims 6, 8, 10, 18, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rierden in view of U.S. Patent 6,374,296 by Lim et al. (Lim).

With respect to Claim 6, Rierden teaches all the limitations of Claim 2 but does not explicitly disclose the use of ATM cells being sent from the non-blocking switch. However it is well known in the art that ATM can be used for transfer of data as shown by Lim (Col. 6 lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the system disclosed by Rierden and modify it as indicated by Lim with the intelligent switch receiving messages from the non-blocking

switch in the form of ATM cells. One would be motivated to have this since it is desired in implementing networks to use Industry standards such as ATM, Ethernet, and TCP (Col. 5 line 65 to Col. 6 line 11).

With respect to Claim 8, Rierden teaches all the limitations of Claim 7 but does not explicitly teach the file transfer is in accordance with a TCP named file transfer protocol. However, it is well known in the art that files can be transferred using a TCP named file transfer protocol as found in the standard ISO protocol suite as shown by Lim (Col. 6 lines 6-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the system disclosed by Rierden and modify it as indicated by Lim wherein the file transfer is performed in accordance with a TCP named file transfer protocol over an identified connection. One would be motivated to have this since it is desired in implementing networks to use Industry standards such as ATM, Ethernet, and TCP (Col. 5 line 65 to Col. 6 line 11).

With respect to Claim 10, Rierden teaches all the limitations of Claim 1 but does not explicitly teach the set of specialized handler processors includes a processor including computer gateway interface (CGI) functionality. However it is well known in the art that one can include CGI functionality in a specialized handler that will process a user request as shown by Lim (Col. 9 lines 10-12).). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the system disclosed by Rierden and modify it as indicated by Lim wherein the set of specialized handler processors includes a processor including computer gateway interface (CGI) functionality. One would be motivated to have this since CGI functionality is common in

the web server environment and aids in determining and dynamically processing a user's request (Col. 8 line 67 to Col. 9 line 9).

With respect to Claim 18, Rierden teaches all the limitations of Claim 14 but does not explicitly disclose the use of ATM cells being sent from the non-blocking switch. However it is well known in the art that ATM can be used for transfer of data as shown by Lim (Col. 6 lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the method disclosed by Rierden and modify it as indicated by Lim with receiving, by the intelligent switch, a message from the non-blocking switch in the form of ATM cells. One would be motivated to have this since it is desired in implementing networks to use Industry standards such as ATM, Ethernet, and TCP (Col. 5 line 65 to Col. 6 line 11).

With respect to Claim 20, Rierden teaches all the limitations of Claim 19 but does not explicitly teach the file transfer is in accordance with a TCP named file transfer protocol. However, it is well known in the art that files can be transferred using a TCP named file transfer protocol as found in the standard ISO protocol suite as shown by Lim (Col. 6 lines 6-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the method disclosed by Rierden and modify it as indicated by Lim wherein the processor facilitating transfer of a file operates in accordance with a TCP named file transfer protocol over an identified connection. One would be motivated to have this since it is desired in implementing networks to use Industry standards such as ATM, Ethernet, and TCP (Col. 5 line 65 to Col. 6 line 11).

With respect to Claim 22, Rierden teaches all the limitations of Claim 13 but does not explicitly teach the set of specialized handler processors includes a processor including computer gateway interface (CGI) functionality. However it is well known in the art that one can include CGI functionality in a specialized handler that will process a user request as shown by Lim (Col. 9 lines 10-12).). It would have been obvious to one of ordinary skill in the art at the time the invention was made to take the method disclosed by Rierden and modify it as indicated by Lim providing, within the set of specialized handler processors, a processor including computer gateway interface (CGI) functionality. One would be motivated to have this since CGI functionality is common in the web server environment and aids in determining and dynamically processing a user's request (Col. 8 line 67 to Col. 9 line 9).

(10) Response to Argument

The examiner first makes note of the examiner's interpretation of the Rierden reference in relation to the claimed subject matter as it is pertinent to understanding the examiner's responses to the arguments.

Particularly important to the issues of the appeal brief is the subject matter related to the "default handler processor" claimed in both independent claims 1 and 13. Rierden discloses a Data Directory Servers (DDS) structure, with details of such a structure beginning in Col. 6. The DDS includes several event handlers including the RPC handler (Col. 7 lines 15-20), which the examiner interprets as being the "default

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handler processor". The RPC handler processes the majority of requests and determines which data server (what the examiner considers to be "specialized handler processors") should server a request based on the type of the request (Col. 16 line 65 - Col. 17 line 24). The Office Action mailed 11/12/03 (Paper #3) proposes a logical separation of the RPC handler functionality from the DDS such that the RPC handler is the default handler processor and the remaining DDS functionality serves as the intelligent switch connected to the network interface. This logical separation is supported by Col. 16 line 65 - Col. 17 line 5 as it states that control is relinquished from the DDS to the RPC handler, thus establishing the RPC handler as a separate functional block from the rest of the DDS structure.

The specific arguments will now be addressed.

With respect to Claim 1 (arguments on Pages 4-5 of the Appeal Brief):

Appellants' argument A: On Page 4, last paragraph, of the Appeal Brief, Appellants argue that the limitation, "without intervention by the default handler processor", *"does not entail the "pass through" mode described in Rierden since the act of passing the results through the DDS consumes processor assets (bus cycles, memory, etc.)."*

Examiner's response: Appellants offer no evidence from Rierden as to why the DDS would consume processor assets as stated by Appellants. On the contrary, Rierden actually states in Col. 9, lines 22-25,

"Alternatively, the result set may pass through the DDS 150 to the client 120 without any additional processing on the part of the DDS 150. The latter situation is generally termed "pass-through mode"." (emphasis added)

It is clear from this that the result set is NOT passed back to the RPC handler (the "default handler processor") or any other functional part of the DDS for further processing. The DDS only serves as part of a direct communication path to the requestor. This is further evident from Col. 17, lines 16-18, where Rierden states that in "pass through" mode (also referred to as passthru or pass thru by Rierden), results of a request *"pass thru the intermediate DDS directly to the client."* This is similar to the Appellants' description in the specification. Particularly, on page 32, lines 1-3, the specification states that the "specialized handler processors" are delegated requests and further communicate *"directly to the requestor on the connection associated with the delegated request without intervention by the default network processor 16."*(emphasis added).

Appellants' argument B: On Page 4 of the Appeal Brief, last paragraph, Appellants further argue the appropriate definition for "intervene" is "to come, be, or lie between", in view of the disclosure.

Examiner's response: No details are given as to how the disclosure necessarily presents such a view. Nonetheless, taking this definition into consideration, the teachings of Rierden are still within the scope of "without intervention". As described above, Rierden states that the "pass-through mode" allows the result of a

request to pass through the DDS without any additional processing (Col. 9 lines 22-25). While the DDS is interposed between the network interface and the servers that carry out the request, the RPC handler (the default handler processor) does not receive the results in pass through mode. This is further evident in Col. 17, lines 43-49, which states that if a request was an "ALL" request, then the results may be returned to the RPC handler process flow. However, this section makes the distinction that if the request was not an "ALL" request, then "the result sets are returned to the requesting client in passthru mode through the DDS". In other words, it does not return to the RPC handler process flow in the case of pass through mode. As such, the RPC handler processor does not "come, be, or lie between". Therefore, Rierden's teachings are within the scope of and anticipate "without intervention by the default handler processor".

Appellants' argument C: On page 5 of the Appeal Brief, the Appellants argue the "logical" separation of the RPC handler function from the DDS "ignores structural elements described in the specification and recited in claim 1 - in particular, physically separating the intelligent switch (for routing communications between the processors and the network interface) from the default handler processor."

Examiner's response: The claim language only states "a default handler processor coupled to the intelligent switch". What the examiner proposes with the logical separation of the RPC handler functionality is that which is akin to the Appellants showing in Fig. 1. Particularly, Fig. 1 shows a high level block diagram of the primary

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components, including the default handler processor (16) and the intelligent switch (24). Both these components are grouped together on the same Network Processor (10). In the Rierden reference, the logical separation of the RPC handler is asserting the RPC handler can be represented as a high level block that is part of the overall DDS structure.

Appellants' argument D: On page 5 of the Appeal Brief, in the last paragraph for arguments directed to claim 1, Appellants argues

"Rierden's does not disclose that the recited "bus structure" and "request reassignment tracking logic" enable completing subsequent communications between the handler processors (data servers 160) and the network interface (105) 'without intervention by the default handler processor' (DDS 150)".

Examiner's response: The examiner notes that the claimed subject matter regarding the recited "bus structure" and "request reassignment tracking logic" does not enable completing subsequent communications between the handler processors and the network interface "without intervention by the default handler processor". The claimed subject matter states "facilitating completing at least the portion of the new request" (from Claim 1), not enabling completion of subsequent communications. This was also noted in the Final Rejection mailed 6/22/04 (page 13). Furthermore, the examiner has not interpreted the DDS of Rierden to be the default handler processor. The RPC handler is interpreted by the examiner, to be the default handler processor. As described above, the RPC handler does not receive the results in pass through

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mode and therefore does not “intervene” between the specialized handler processors (data servers in Rierden) and the requesting client. The results are communicated directly to the requesting client. While these communications are sent through the DDS structure, it was also shown that none of the DDS structure, including the RPC handler, will perform additional processing on these results in pass through mode. As such, the “bus structure” and “request reassignment tracking logic” taught by Reirdon, enable facilitating completing at least the portion of the new request “without intervention by the default handler processor”, and are therefore within the scope of the claimed subject matter.

With respect to Claim 13 (arguments on pages 5-6 of the Appeal Brief):

Appellants’ argument E: Starting on Page 5 and continuing to Page 6, the Appellants argues that pages 14–15 of the Final Office Action (6/22/04) “does not acknowledge that claim 13 calls for communications between the identified handler and the network interface while executing a *portion of the new request* and bypassing the default handler processor while executing *the portion of the new request*”.

Examiner’s response: The examiner is unsure as to how this was not acknowledged. The following is taken directly from pages 14-15 of the Final Office Action (6/22/04):

“The exact claim limitation of concern from Claim 13 is as follows: “executing, by the identified handler processor, at least the portion of the new request, wherein during the executing step the identified handler processor communicates with the network interface via the intelligent switch; thereby bypassing the default handler

processor while executing at least the portion of the new request.” Rierden shows that the identified handler processor executes at least the portion of the new request. **Specifically, Rierden states the specialized handlers (data servers) execute the RPC’s (Col. 7 lines 65-67) which are part of a new request (Col. 16 lines 65-67).** After the RPC handler has identified the appropriate handler, part of the execution of the RPC requires the DDS to communicate with the identified handler to check for and establish a connection as needed (Col. 17 lines 40-43). Therefore, Rierden does disclose an intelligent switch, bus, and multiprocessor arrangement that would support the recited steps including “bypassing the default handler processor while executing at least a portion of the new request.”” (emphasis added)

This citation provides a clear explanation of the execution of “a portion of the new request” in light of the claim language.

Appellants’ argument F: On page 6, in the last paragraph of arguments directed to claim 13, Appellants argue that Rierden does not disclose a non-blocking switch and assert that an unduly broad interpretation of “non-blocking” was given.

Examiner’s response: Appellants state “non-blocking should be given its ordinary, clear meaning”, yet do not describe in detail the “ordinary, clear meaning” of ‘non-blocking’. Nor does the specification provide any details as to how one would define ‘non-blocking’ in relation to the claimed subject matter. From page 15 of the Final Office Action (6/22/04), the following interpretation of non-blocking was given:

“The examiner interprets a non-blocking switch as having the capability of providing access to resources without the client having to wait due to congestion/traffic at the switch due to a large number of client requests. This is

one of the problem Rierden addresses (Col. 1 lines 13-50), and the DDS in Rierden accesses resources for a multiple concurrent client requests in processing large numbers of transactions. Therefore, the examiner interprets Rierden to disclose a non-blocking switch interposed between a DDS and the data servers.”

The examiner asserts this described capability is within the “ordinary, clear meaning” since the client will not be blocked (ie. have to wait due to congestion/traffic) when making requests to the system, even when there are a large number of client requests being made to the system.

With respect to Claims 11 and 23 (Argument on page 6 of the Appeal Brief):

Appellants’ argument G: Appellants argue there is no basis in the cited references for the examiner’s proposed teachings of the recited claim structure of claims 11 and 23 (page 6 of the Appeal Brief).

Examiner’s response: While Appellants do not specifically state the structure at issue, the examiner assumes the structure at issue is the “data retrieval buffer” cited in both claims. As stated in the Final Office Action (6/22/05), page 16, Rierden specifically states that the data storage facilities should typically be implemented as SQL devices (Col. 7 lines 65-67). The examiner asserts that one of ordinary skill in the art would know that SQL devices, contain a buffer (usually referred to as a buffer cache or data cache) for storing the most recently retrieved data. Therefore, Rierden anticipates such a structure. Rierden also teaches the data server may be composed of a processor and the database (Col. 5 lines 2-5). Based on the knowledge that SQL devices contain a “data retrieval buffer”, it is inherent, based on its functionality, that this buffer is

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interposed between the processor (specialized processor) and the database (data storage facility).

With respect to Claims 3 and 15 (Argument on page 6 of the Appeal Brief):

Appellants' argument H: Appellants state an inability to discern any suggestion to incorporate the secondary reference's (Basham) teachings into the system disclosed in Rierden and assert such an inability was previously submitted (page 6 of the Appeal Brief).

Examiner's response: The examiner responded to this previous submission on pages 16-17 of the Final Office Action (6/22/04). Furthermore, the rejection of Claims 3 and 15 in the Final Office Action (6/22/04), pages 6-7, provide a clear prima facie case, which explicitly includes a motivation statement. Basham suggests the use of version controlled partitions for data storage (Col. 4 lines 39-42 of Basham) and provides motivation as to why one would use version controlled partitions in a data storage facility, such as those in Rierden. Particularly, there is need to share data among multiple clients without destroying the integrity of the data (Col. 1 lines 33-36 of Basham). Appellants have provided no response to the prima facie case or the examiner's response to arguments presented in the Final Office Action (6/22/04), other than a conclusive statement with no explicit reasoning or evidence.

With respect to Claims 4 and 16 (Argument on page 7 of the Appeal Brief):

Appellants' argument I: Appellants argue the combination of Rierden in view of Basham and Jacobson does not teach the recited structure nor provide any teaching to modify (page 7 of the Appeal Brief).

Examiner's response: This argument was also previously submitted and addressed by the examiner in the Final Office Action (6/22/04) on page 17. Furthermore, the rejection of Claims 4 and 16 in the Final Office Action (6/22/04), pages 7-8, provide a clear prima facie case, which explicitly includes a motivation statement. Jacobson specifically teaches a section in memory (a "straddle") is used for temporary storage during a relocation data (Col. 8 lines 30-39 of Jacobson). The purpose is for the continuous availability of the data while this operation is being performed (Col. 9 lines 36-44 of Jacobson) which is a desired feature (Col. 1 lines 30-40 of Jacobson). Therefore the combination of Rierden, Basham and Jacobson discloses "using the recited multiprocessor architecture to provide access to a data storage facility that supports incorporating a straddle into storage partitions to facilitate copying stored data assets while maintaining the availability of the stored asset while the data is being copied to a new location." Appellants have provided no response to the prima facie case or the examiner's response to arguments presented in the Final Office Action (6/22/04), other than a conclusive statement with no explicit reasoning or evidence.

With respect to Claims 5 and 17 (Argument on page 7 of the Appeal Brief):

Appellants' argument J: Appellants argue the combination of Rierden in view Rungta does not teach the recited structure nor provide any teaching to modify (page 7 of the Appeal Brief).

Examiner's response: This argument was also previously submitted and addressed by the examiner in the Final Office Action (6/22/04) on page 18. Furthermore, the rejection of Claims 5 and 17 in the Final Office Action (6/22/04), pages 8-9, provide a clear prima facie case, which explicitly includes a motivation statement. Rungta specifically discloses the use of bit-map entries that represent the current state of files within a data storage facility (Col 1 lines 42-54 of Rungta). Rungta further discloses there is need for internal file consistency in maintaining a system (Col. 1 lines 25-26 of Rungta). Appellants have provided no response to the prima facie case or the examiner's response to arguments presented in the Final Office Action (6/22/04), other than a conclusive statement with no explicit reasoning or evidence.

With respect to Claims 6, 8, 10, 18, 20 and 22 (Argument on page 7 of the Appeal Brief):

Appellants' argument K: Appellants argue the combination of Rierden in view Lim stating that the Final Action "*does not identify the teachings in the cited references that suggest their combination to render the claimed invention*" (page 7 of the Appeal Brief).

Examiner's response: A similar argument was also previously submitted and addressed by the examiner in the Final Office Action (6/22/04) on page 18. In the

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Appeal Brief, Appellants state *"Appellants respectfully submit that while each of the elements, by themselves, may be known, the prior art does not disclose or suggest incorporating the recited elements into a system including the multiprocessor architecture recited within each of these claims"*. Appellants have not identified what elements they are referring to, nor have they provided any reasoning as to why the citations provided in the rejection presented in the Final Office Action (6/22/04), pages 9-12, for each of these claims does not teach the claimed subject matter. The rejection of each of these claims provides a clear prima facie case, explicitly including a motivation statement. The examiner is at a loss as to how the Appellants could not identify the teachings, which are clearly cited in each rejection. Appellants have provided no response to the prima facie case or the examiner's response to arguments presented in the Final Office Action (6/22/04), other than a conclusive statement with no explicit reasoning or evidence.

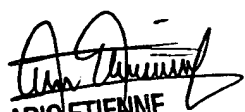
For the above reasons, it is believed that the rejections should be sustained.

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Respectfully submitted,



David Lazaro
June 21, 2005



ARIO ETIENNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100



SALEH NAJJAR
PRIMARY EXAMINER

Conferees
Saleh Najjar
Ario Etienne
Technology Center 2100

LEYDIG VOIT & MAYER, LTD
TWO PRUDENTIAL PLAZA, SUITE 4900
180 NORTH STETSON AVENUE
CHICAGO, IL 60601-6780